Scalable MoS_2 phototransistors with ultra low power consumption and high light/dark current ratios

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Outline

1- Introduction

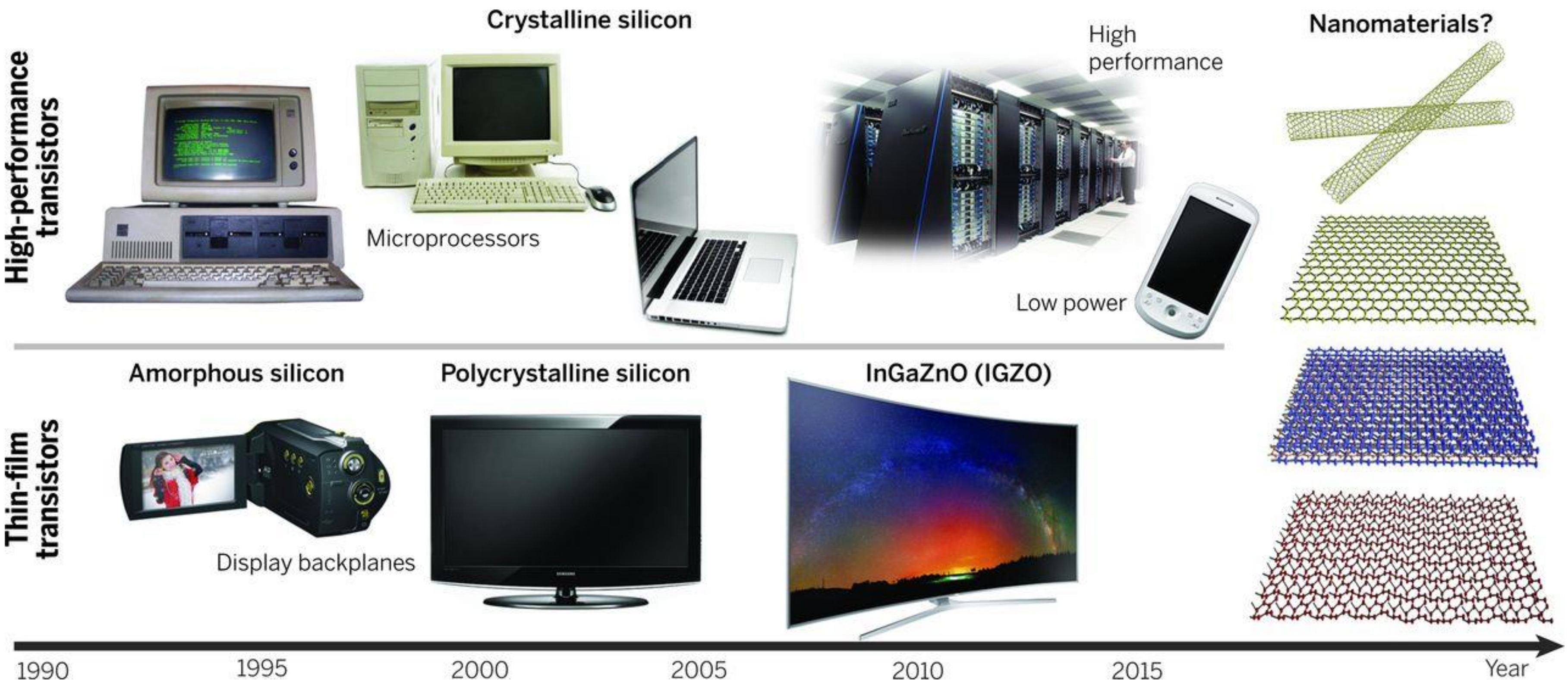
1.1 Background
1.2 Material selection
1.3 Schematic of our devices

2- Fabrication and characterization

2.1 Fabrication
2.2 Output characteristic curves
2.3 Transfer characteristic curves

3- Discussion and summary

1.1 Background

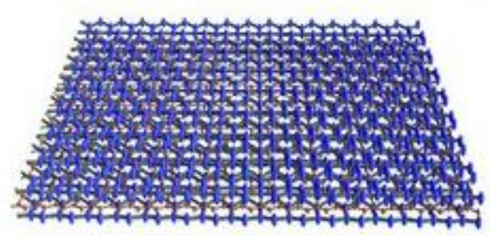


Technologies enabled by high-performance and thin-film transistors over the past 25 years.

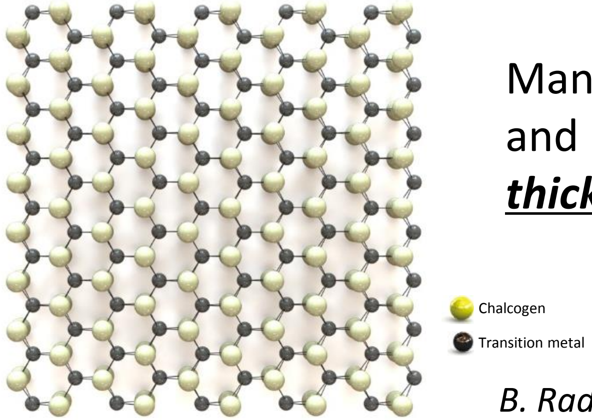
A. D. Franklin, Science, 349(6249), abb2750 (2015)

1.2 Introduction (material selection)

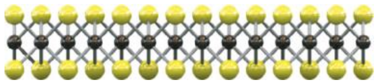
1. Semiconductor
2. Sizable energy band gap
3. Band gap changes with increasing number of layers



A. D. Franklin, Science, 349(6249), abb2750 (2015)

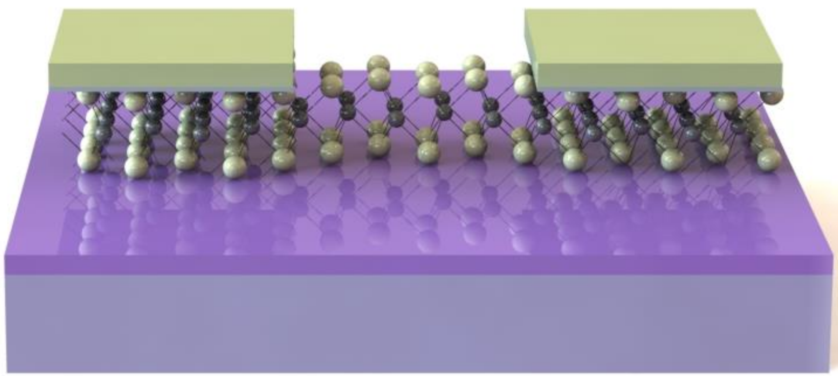


Many combinations of transition metals and chalcogens can yield the ***three-atom-thick*** arrangement of a monolayer TMD.



B. Radisavljevic et al., Nat. Nanotechnol., 6, 147-150 (2011)

1.3 Schematic



X. Jing, M. Lanza et al., Nano Energy (2016)*
http://dx.doi.org/10.1016/j.nanoen.2016.10.032

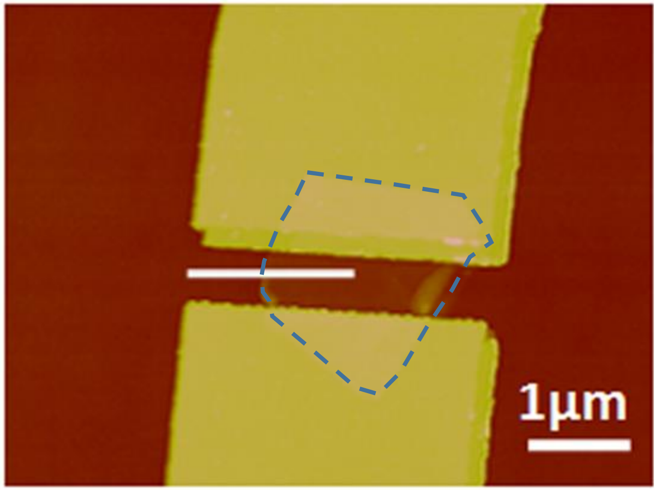
MoS_2 → CVD grown single layer

Contacts → Photolithography

Channel → W = 20 µm, L = 40 µm

Single back gate (SiO_2 = 300 nm)

Our advantage is that we use CVD-grown MoS_2 and photolithography, meaning that (unlike exfoliated prototypes using electrodes patterned by electron beam lithography) **our devices are scalable.**



Li et al., Appl. Phys. Lett. 105, 093107 (2014)

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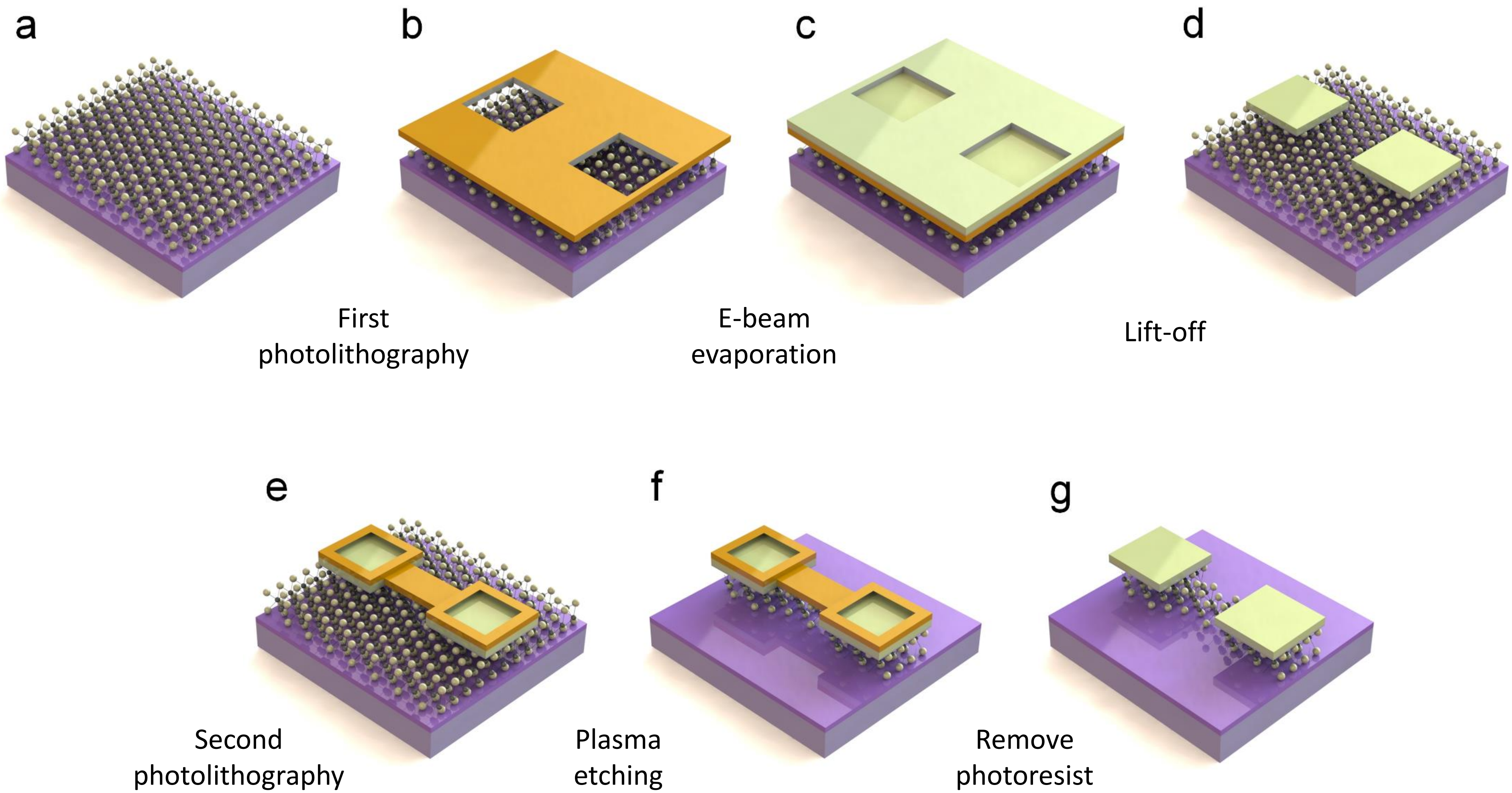
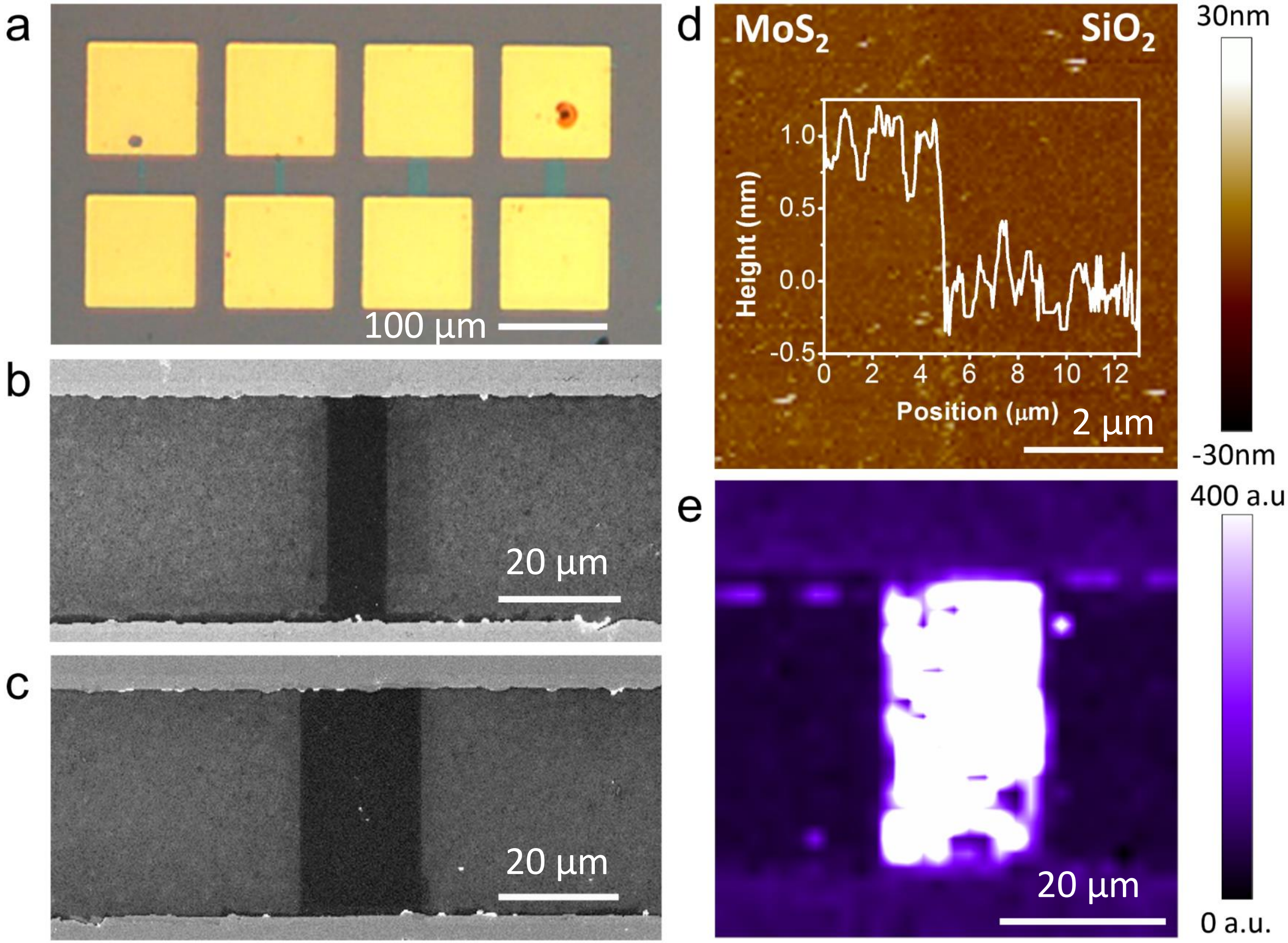
2.1 Process of fabricating MoS_2 phototransistor



X. Jing, M. Lanza et al., Nano Energy (2016)*
http://dx.doi.org/10.1016/j.nanoen.2016.10.032

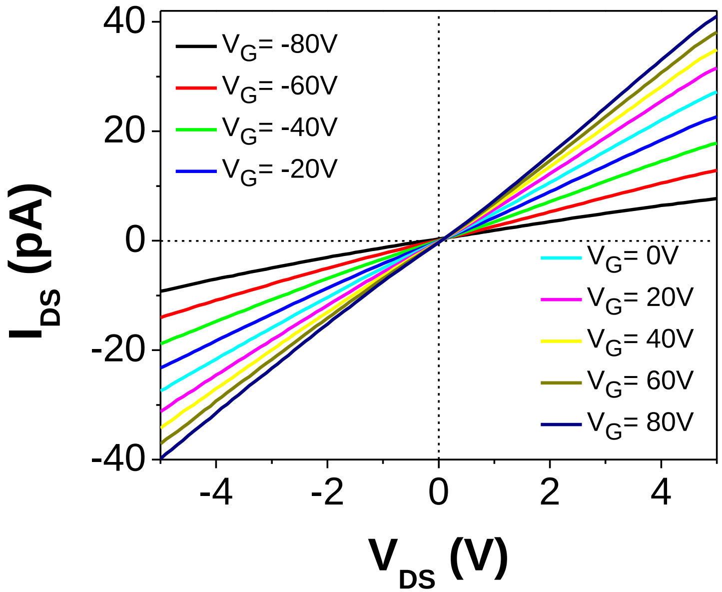
2.1 Optical and SEM images; AFM and Raman maps



X. Jing, M. Lanza et al., Nano Energy (2016) http://dx.doi.org/10.1016/j.nanoen.2016.10.032*

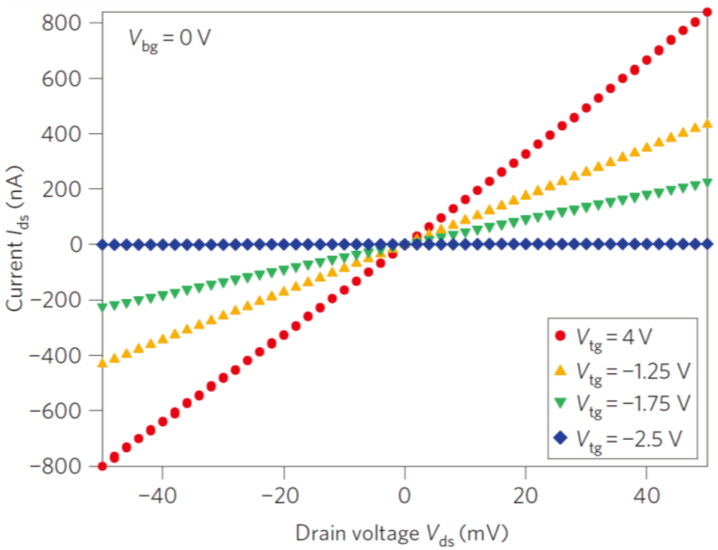
2.2 Output characteristics (W= 20µm)

As-fabricated



X. Jing, M. Lanza et al., Nano Energy (2016)*
http://dx.doi.org/10.1016/j.nanoen.2016.10.032

From literature



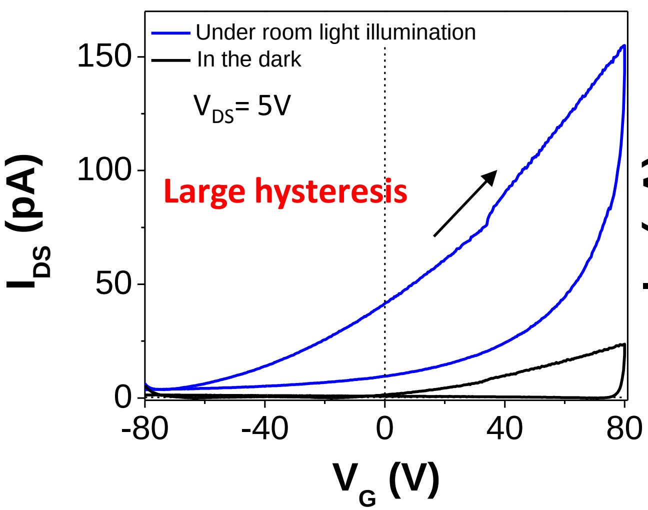
Radisavljevic et al., Nat. Nanotechnology, 6, 147-150 (2011)

As it can be observed, **I_{DS} depends linearly on V_{DS}** and **the curves are quasi-symmetric with respect to the origin**, indicating the formation of Ohmic contacts between Au/Ti electrodes and the MoS_2 channel.

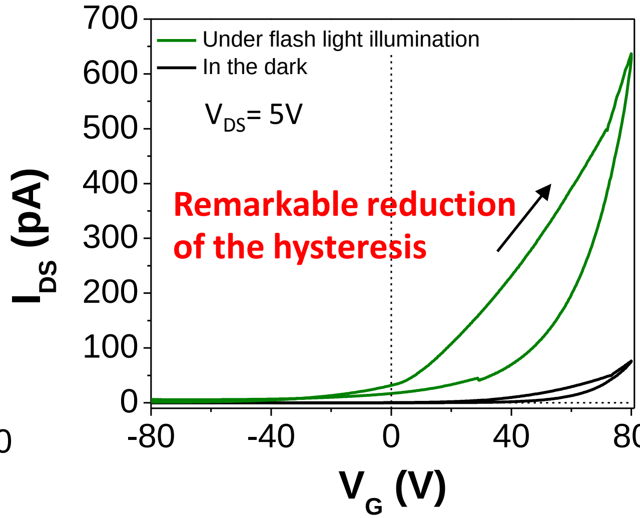
Our devices show typical FET behavior, as previously reported.

2.3 Transfer characteristics (W= 20µm)

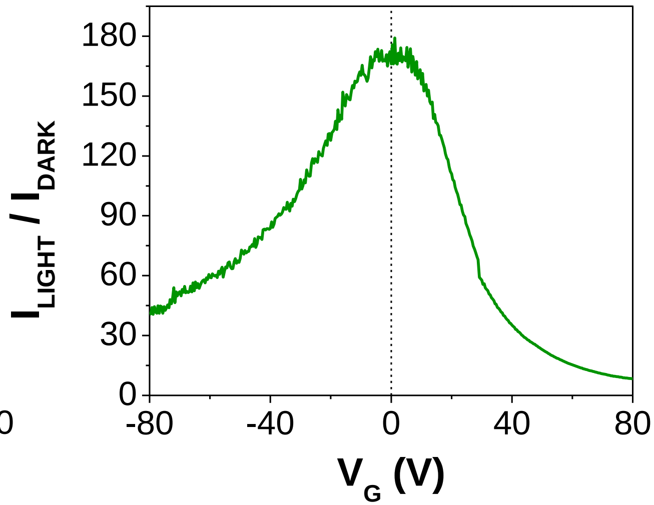
As-fabricated



After annealing



I_{LIGHT}/I_{DARK} ratio



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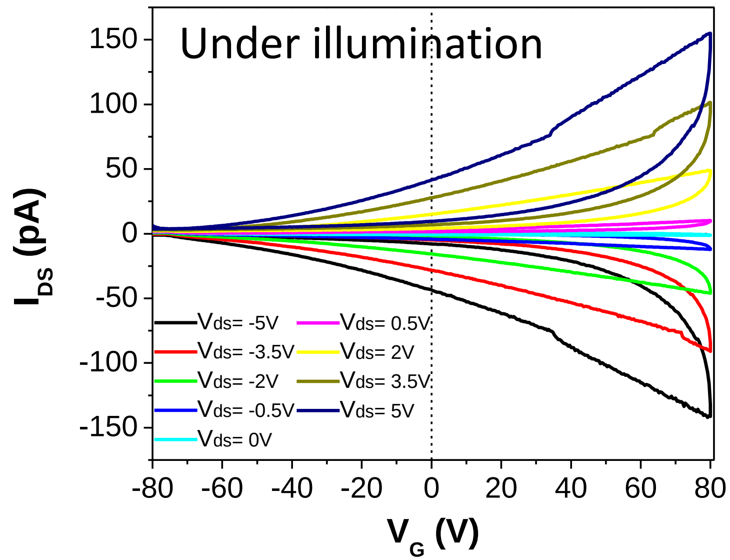
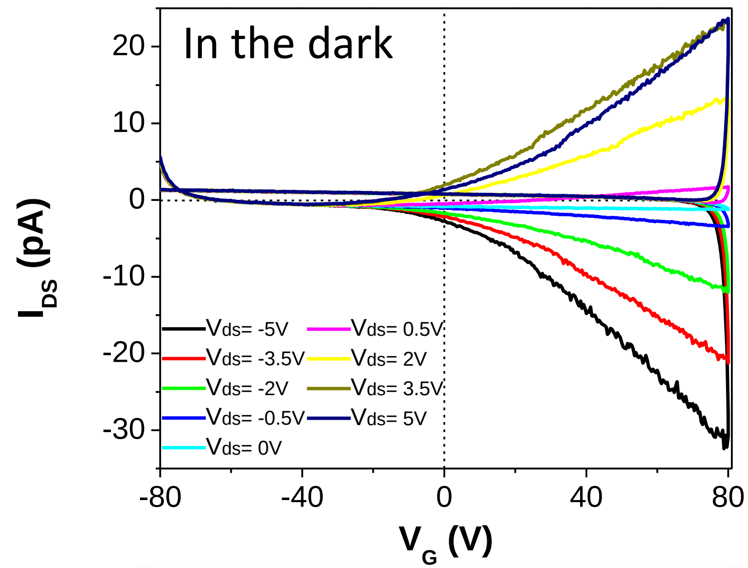
<u>The current of our sample under illumination is much higher than the current in the dark.</u>

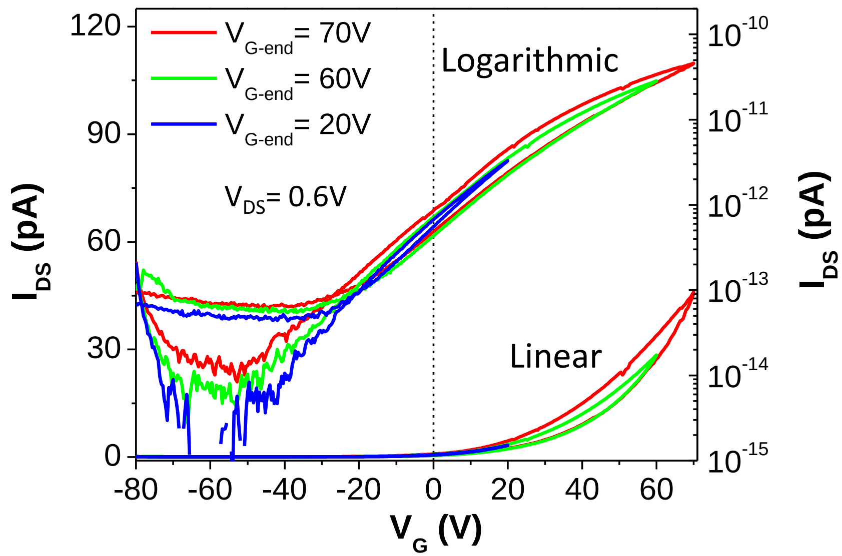
Our devices also show significant photosensitivity, as previously reported.

The ratio at 0 V is 170, which is highest we can find from previous literatures.

2.3 Transfer characteristics (W= 20µm)







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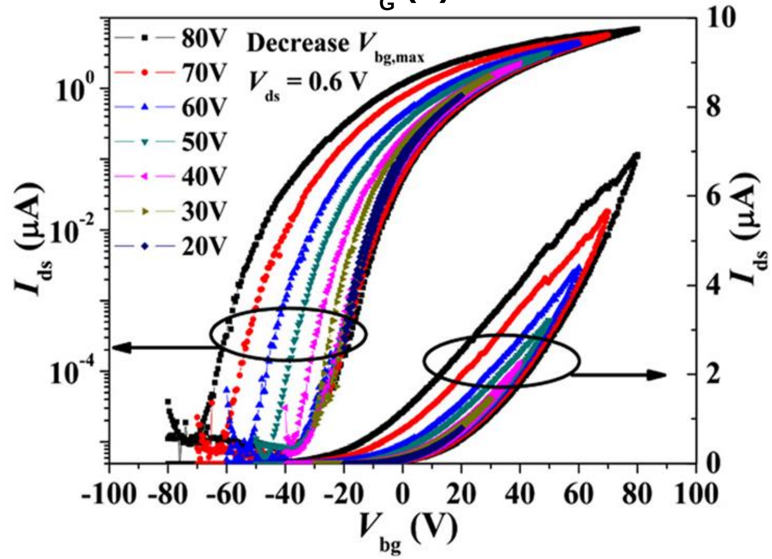

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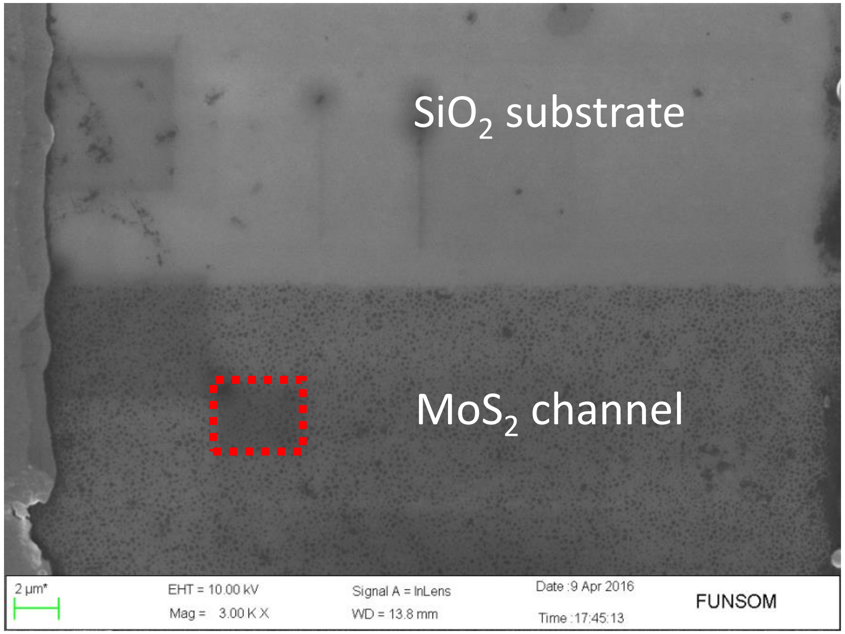
3.1 Comparison of results

Our samples	*Li et al., Appl. Phys. Lett. 105, 093107 (2014)*	*Radisavljevic et al., Nat. Nanotechnology, 6, 147-150 (2011)*	*Late et al., ACS Nano, 6(6), 5635–5641 (2012)*	*Najmaei et al., Nature Materials, 12, 754-759 (2013)*	*Yin et al., ACS Nano, 6(1), 74-80 (2012)*	*L.S. et al., Nat. Nanotechnology, 6, 497-501 (2013)*
CVD grown single layer MoS_2	7-8 layers exfoliated MoS_2	Mechanical exfoliated (single layer)	CVD grown single layer MoS_2	CVD grown (thickness unclear, seems to be single layer)	Mechanical exfoliated (single layer)	Mechanical exfoliated (single layer)
Contacts → Photolithography	Contacts → Electron beam lithography	Contacts → Electron beam lithography	Contacts → Electron beam lithography	Contacts → Photolithography	Contacts → Photolithography	Contacts → Electron beam lithography
Channel → W = 20 um , L = 40 um L/W ratio = 2	Channel → W = 1.5 um , L = 0.6 um L/W ratio = 0.4	Channel → W = 4.5 um , L = 1.5 um L/W ratio = 0.33	Channel → W = 2-10 um , L = 1 um L/W ratio = 0.5 to 0.1	Channel → W = 10 um , L = 100 um L/W ratio = 10	Channel → W = 2.6 um , L = 2.1 um L/W ratio = 0.81	Channel → W = 2 um , L = 1 um L/W ratio = 0.5
Single back gate (SiO_2 = 300 nm)	Single back gate (SiO_2 = 320 nm)	Top gate (SiO_2 = 270 nm)	Single back gate (SiO_2 = 300 nm)	Single back gate (SiO_2 = 285 nm)	Single back gate (SiO_2 = 300 nm)	Single back gate (SiO_2 = 270 nm)
At ambient environment / in the vacuum	A shielded probe station	A home-built shielded probe station	At room temperature in air	Under the vacuum		
Different illumination condition	No mention the light	No mention the light	under uniform white illumination (radiant flux density ~0.7 mW cm^{-2})	No mention the light	Optical power of light = 80 μW	Illumination power is 0.15 mW
Ohmic contact	Ohmic contact	Ohmic contact	Ohmic contact			
	Mobility = 12.66 $cm^2 V^{-1} s^{-1}$		Mobility = 1.1 to 10 $cm^2 V^{-1} s^{-1}$	Mobility = 4.27 $cm^2 V^{-1} s^{-1}$		
I_{LIGHT}/I_{DARK} = 170			I_{LIGHT}/I_{DARK} = 4		I_{LIGHT}/I_{DARK} = 1.75	I_{LIGHT}/I_{DARK} = 4
$V_{DS} \times I_{DS}$ under the light = 3.25×10^{-9}W			$V_{DS} \times I_{DS}$ under the light = 1.6×10^{-5}W		$V_{DS} \times I_{DS}$ under the light = 1.7×10^{-8}W	$V_{DS} \times I_{DS}$ under the light = 3.0×10^{-6}W

3.2 Origin of the small current: small domain size

The origin of the small currents in our devices (compared to the literature) is the role of the grain boundaries in the MoS_2



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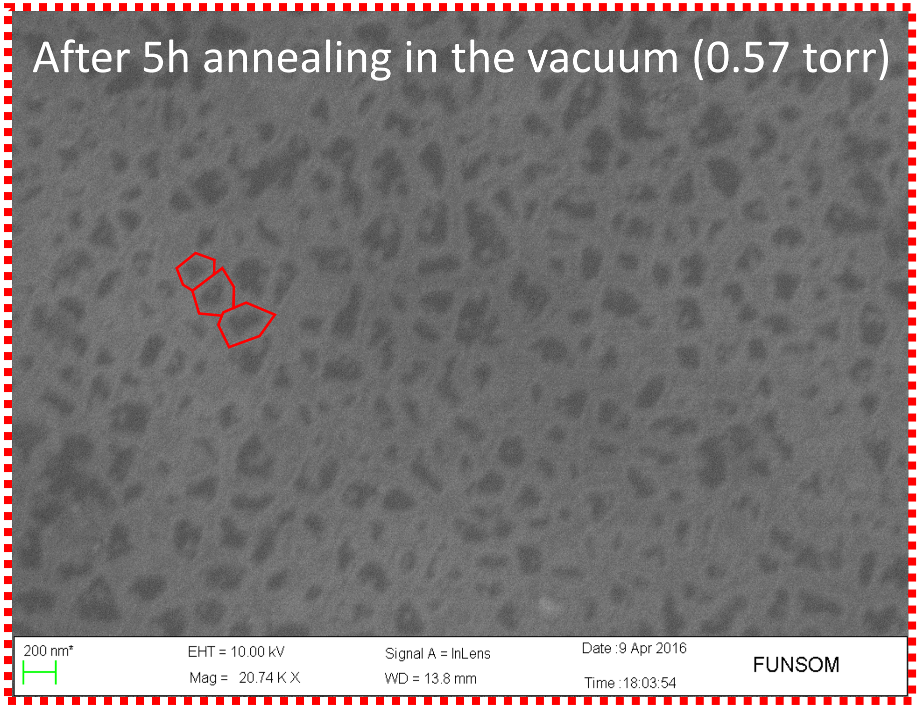

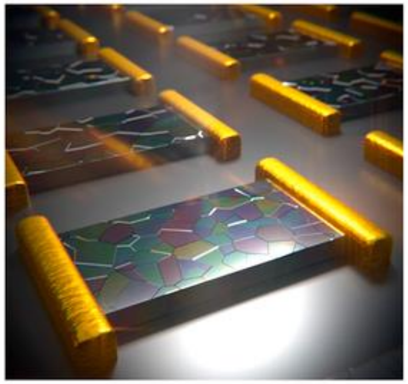

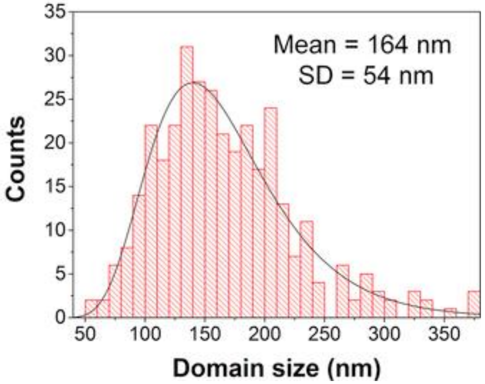

3.3 Conclusions

• We successfully fabricated MoS_2 transistors only using **scalable techniques** (CVD + photolithography; no transfer process needed).

• The transistors show **ultra low power consumption** (3.25×10^{-9} W) due to the large density of grain boundaries in the MoS_2 (small domains, and large amounts of domain boundaries).

• The devices can also work as **photodetectors**. The **I_{Light}/I_{Dark} ratios (170) are larger** than those in the literatures, and they show to be stable over the time.

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